Design and Performance of the 5 GHz Waveform Digitizing Chip DRS3

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***Abstract*– The DRS3 chip is a radiation hard switched capacitor array (SCA) fabricated in a 0.25 µm CMOS process. It features 12 channels with 1024 bins each at a sampling rate of up to 5 GHz. Its signal-to-noise ratio is equivalent to 11.5 bits and the integral nonlinearity is 0.5 per mille with a temperature coefficient below 50 ppm per degree C. A special readout mode can be used to digitize only a certain region of interest from the waveform, bringing down the readout time to 3 µs for a signal which is hundred samples wide. The high channel density and superior electrical characteristics allow for new experiments with excellent pile-up rejection and pulse shape discrimination, while simultaneously eliminating the need for conventional ADCs and TDCs.**

I. Introduction

MODERN trends in data acquisition in particle physics go to higher event rates and therefore suffer more and more from pile-up problems. Furthermore, advanced techniques like particle identification through pulse shape analysis or event-by-event baseline estimation require the acquisition of detector waveforms at high sampling rates. Thus leads to the usage of flash ADCs (FADC) with sampling rates in the typical range from 50 to 250 MHz with 10 or 12 bits of resolution. While such FADCs become more and more common, they suffer from high power requirements, low channel densities and are usually expensive. An alternative approach is to use switched capacitor arrays (SCA). These ASICs sample the input signal in a series of capacitors at high sampling rates, and are then read out at lower frequencies through a shift register with commercial ADCs. The sampling frequency is generated with an on-chip inverter chain ("domino chain"), thus eliminating the need to generate clock signals in the GHz range (Fig. 1).

Several such ASICs have been developed for particle physics applications, for example [2] and [3]. This paper presents such a chip developed for the MEG Experiment [1] at PSI, Switzerland. Since the domino wave runs continuously in a ring the chip is called Domino Ring Sampler (DRS). The DRS3 chip is the third generation of a series of developments started in 2001. Care has been taken in the design of the chip not to implement any features only specific to the MEG experiment, so that the chip can be useful for other applications outside the MEG experiment as well, such as hand-held oscilloscopes for example.

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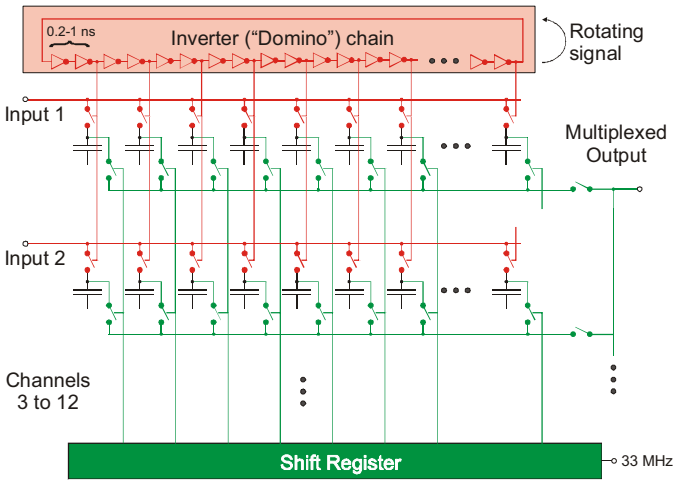

Fig. 1. Schematics of a SCA with an inverter chain, a series of sampling capacitors for several channels, and a shift register for the readout of the capacitors through a multiplexed output.

II. Architecture

A. Inverter Chain

A potential problem of the inverter chain is the non-linearity one observes if the domino wave reaches the end and wraps around to the beginning. Depending on the chip layout, a sampling gap of several bins might occur. To prevent this, the DRS3 chip uses a folded architecture, where the inverter chain is divided into two equal parts, with one part running from left to right and the second part running from right to left. The layout has been careful optimized at the transition points such that a highly linear domino wave is generated.

The usual architecture of an inverter chain uses an odd number of inverters, like it is found on most voltage controlled oscillators (VCO). A zero-to-one transition propagates through the complete chain, followed by a one-to-zero transition. Sine PMOS and NMOS transistors can never be matched perfectly, there would always be a slight timing difference between the two transitions when opening the write switches to the sampling capacitors. The DRS3 chip uses instead of two inverters two NAND gates as depicted in Fig. 2. A short pulse at the `Start` input ignites the domino wave in domino cell 1, which then travels from left to right and opens the write switch of each sampling cell at its `Sampling Cell` output. The PMOS transistor at the output of the second NAND gate in every cell is made much stronger than its NMOS counterpart, which leads to a widening of the pulse over time. A feedback signal from the following cell "cuts" the end of this pulse to keep its width constant over time ("tail biting"). To control the

speed of the domino wave, a variable resistor made out of a transition gate is placed between the cells, which forms together with the parasitic input capacitance of each cell a RC delay circuit. The sampling speed can therefore varied in a wide range by means of an external control voltage V_{speed}. The domino wave can be stopped by lowering the `Enable` line. This has however the disadvantage that the last domino cell might send a shortened write pulse to its sampling cell. To prevent this, an additional latch is placed in each domino cell. It latches the status of the `Write` signal when the domino wave passes through the cell, and gets reset when the wave reaches the following cell. If the sampling process is now stopped by lowering the `Write` line, all signals sent to the sampling cells are guaranteed to have the same width.

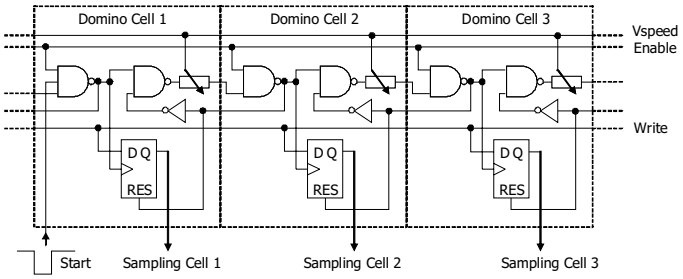

Fig. 2. Simplified schematics of three out of 1024 domino cells.

The input of the latch reset is actually not taken from the following cell, but from each 16th cells down the chain. This leads to a with of the write pulse of 3 ns at 5 GHz sampling speed, which is enough to charge each sampling capacitor to the current input voltage with an accuracy better than 0.1 mV.

B. Sampling Cell Readout

The readout of the sampling cells imposes quite a challenge. The capacitance of the sampling capacitor is 0.2 pF and therefore much smaller than the parasitic capacitance of any readout bus which is in the order of 20 pF. The direct transfer of this charge off-chip as it was done in the DRS1 chip reduces the signal to a level which is almost impossible to measure. The DRS2 chip therefore uses a NMOS transistor with its gate directly connected to the sampling capacitor. The current flowing though this transistor is proportional to the voltage of the sampling capacitor in some range. It is switched to a readout bus by means of a transition gate and produces a voltage at a common pull-up resistor. While this method works in principle, the current shows a big variation from cell to cell due to the mismatch of the transistors. Furthermore the current strongly depends on the temperature, which requires extended calibration procedures regularly. This has now been solved in the DRS3 chip where each sampling cell contains its own operational transient amplifier (OTA) operated as a buffer (Fig. 3). These OTAs were designed to have a small temperature coefficient and a speed high enough to read out each cell in 30 ns. The challenge was to design them small enough so that more than 12,000 such OTAs fit on a 5x5 mm^2 die. The output of these OTAs is switched to a common readout bus by the readout shift register, and sent off-chip by an additional buffer strong enough to drive a 30 pF external load.

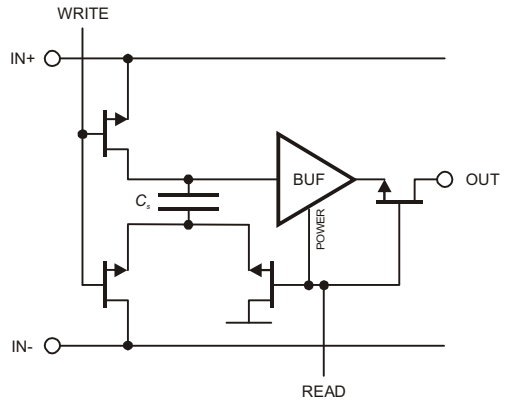

Fig. 3. Simplified schematics of a sampling cell. The write signal comes from the domino cell; the read signal which also powers up the buffer comes from the readout shift register.

C. Region-of-interest readout mode

The inherent problem of SCA chips is the fact that the sampling has to be stopped for data readout. The goal is therefore to minimize this dead time. One step has already been taken in making the readout circuitry fast enough to settle to within 1 mV of the input voltage in 30 ns, making it possible to read out the chip with a 33 MHz clock. The next step was to output all 12 channels either through a multiplexer to a single external ADC or to output all 12 channels in parallel to 12 external ADCs as can be seen in Fig. 5. This reduces the dead time by a factor of 12 compared to the multiplexed readout, with the cost of requiring more external ADCs. An additional reduction in readout time can be achieved by the patented region-of-interest readout mode introduced in the DRS3 chip.

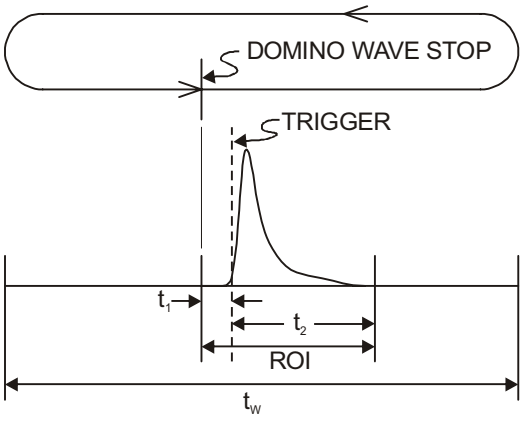

Fig. 4. Region-of-interest (ROI) readout mode. The trigger causing the domino wave stop is delayed externally such that the wave stops just in front of the interesting signal.

In typical particle physics experiments the interesting signal (ROI in Fig. 4) is usually small compared to the whole sampling window t_W. If only this ROI is read out and digitized, a significant reduction in readout time can be achieved. The only problematic point is how to preset the

readout shift register with the correct position. In principle this can be achieved by an external TDC measuring the trigger time, then subtracting an offset and loading the readout shift register with the appropriate position. Since the register can only be loaded serially, this takes time and reduces the benefit from this method. The DRS3 chip performs this operation in a different way. The trigger signal gets delayed externally such that the domino wave gets stopped t_W-t_1 after the trigger point. Then the stop position from the domino cells is transferred internally to the readout shift register in a single clock cycle. The readout starts now at the interesting point and lasts for t_1+t_2. The overall reduction is therefore $(t_1+t_2)/t_W$. If the ROI is for example 100 bins wide, the readout can be performed in (100+1)*30 ns = 3.03 µs.

D. The DRS3 chip

The complete functional block diagram of the DRS3 chip is shown in Fig. 5. The chip is fabricated the 0.25 µm 1P5M MMC process offered by UMC using radiation hard transistors. It contains 12 independent channels each with 1024 bins, which can be combined though a write shift register into 6 channels with 2048 bins, 2 channels with 6144 bins and one channel with 12288 bins. The inputs are sampled differentially, the outputs can be either multiplexed or for all 12 channels in parallel.

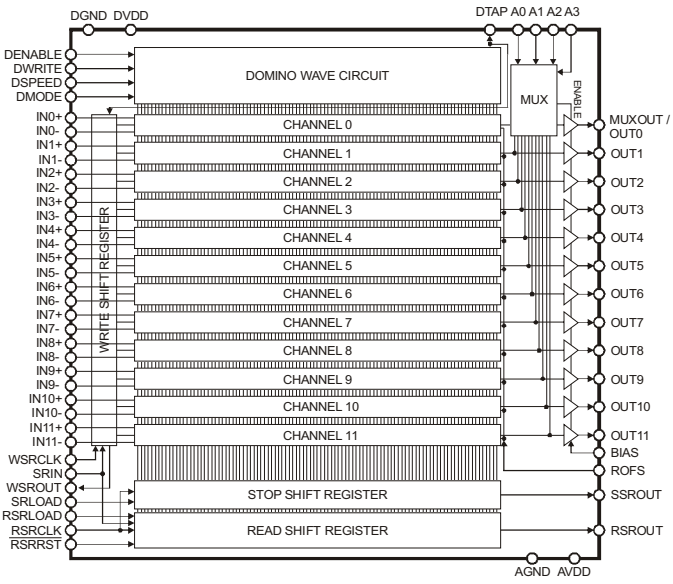

Fig. 5. Functional block diagram of the DRS3 chip

The 5x5 mm^2 die is placed into a 64-pin LQFP plastic package. In the MEG experiment, two chips are combined into a PMC mezzanine card and digitized by a 14-bit FADC AD9248. The mezzanine board can be read out via an USB adapter board, which also supplies the power. We use 8 out of the 12 channels for input data, and two channels to sample an experiment-wide reference clock and the trigger signal, respectively. Two mezzanine boards can be plugged into a general purpose VME board developed at PSI [4], giving a total of 32 channels in a single VME slot.

III. Test Results

The sampling speed is controlled by an analog voltage in the range from 10 MHz to 5 GHz. To stabilize the sampling frequency an external phase-locked-loop (PLL) is used to lock it to a common reference clock which must be 1/2048 of the sampling frequency. A stabilization below 200 ps has been achieved. It must be noted however that there is a cell-to-cell variation of the delay in the domino cell due to the mismatch of the transistors, which can cause an integral time nonlinearity of several ns. This nonlinearity must be measured and corrected for in applications where a timing accuracy below one nanosecond is important.

The analog properties of the DRS3 chip are summarized in Table 1. It should be noted that the bandwidth of 450 MHz is currently limited by the resistance of the analog input bus, and will be increased in the next version also by using a smaller QFN package.

Parameter	**Value**
Noise	5 mV rms 0.35 mV rms (after corr.)
Signal-to-Noise Ratio	69.1 dB
Effective number of bits	11.5
Linear input range	0.1 V – 1.1 V
Integral nonlinearity	0.5 mV
Bandwidth (-3dB)	450 MHz
Crosstalk	< -46 dB
Supply voltage	2.5 V
Supply current	20 mA (1 GSPS, multiplexed readout) 65 mA (5 GSPS, parallel readout)

Table 1. Basic analog parameters of the DRS3 chip

Each cell OTA has a fixed offset with a distribution of 5 mV rms. If these offsets are measured and calibrated for in the readout FPGA, the remaining random noise has an RMS of 0.35 mV, which is equivalent to 11.5 bits resolution at the 1 V input range. The differential signal input helps to reduce the crosstalk below the smallest value the author could measure.

There is however one remaining problem which limits the usage of the DRS3 chip. Assume that a big pulse is sampled and stored in the sampling capacitors, but no trigger happens at this point. Now let's assume that on the next cycle of the domino wave there is no pulse on the input and the stored pulse from the previous cycle is "erased" from the sampling capacitors. While the write signal is wide enough to de-charge the sampling capacitor, there is a build-up of charge on the input bus. This charge must flow back through the input into the low impedance signal source. Since the input bus and the bond wire of the chip do not have zero resistance, there is a certain time constant for this de-charging. Simulations confirmed by measurements have shown that the dynamic equilibrium of capacitors putting their charge back on the input bus and charge absorption by the input source lead to a

significant “residual charge effect”. At 2 GHz sampling speed this effect is of the order of 2%. This means that if a 0.5 V pulse is digitized in one cycle, a “ghost pulse” of 10 mV height will be present if the chip is stopped and read out on the next domino wave cycle. This pulse can mimic for example a wrong PMT hit and is therefore not acceptable in the MEG experiment. The solution of this problem is to add two clear switches to each capacitor, which ground both sides for a few ns just before the write cycle occurs.

IV. Outlook

To implement this solution, it is planned to do one more iteration of the DRS chip. This will also improve the bandwidth and some other analog parameters slightly. The DRS4 chip is currently in the layout phase and will become available in spring 2008. It will be available from our institute also for other experiments. In addition, several companies have announced their interest in building commercial VME boards with the DRS4 chip. An interesting development goes in the direction of combining the DRS4 chip with 8-channel 65 MSPS FADCs such as the AD9222. A DAQ board can then house 32 channels in a single VME slot, which are sampled by the FADC and the DRS4 chip in parallel. Inside the FPGA a trigger decision can be made based on the FADC data, such as a global sum for example. If a trigger occurs, the DRS4 chip is stopped and its output is then digitized through the same FADCs. Therefore the board can be used for triggering and for 5 GHz waveform digitizing at the same time. The waveforms can be analyzed on board to produce charge ADC, peak sensing ADC and TDC data with resolutions below 50 ps.

Acknowledgment

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